Abstract

Briefly, in accordance with one embodiment of the invention, an integrated circuit includes: a gate array architecture. The gate array architecture includes a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions. The diffusion regions have partially overlying polysilicon landing sites to form N-type and P-type transistors. The regions are relatively sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors.